IN THE CLAIMS

Please delete claims 14-17, 19, 25-34 and 38-52 without prejudice or disclaimer.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-9 (cancelled)

Claim 10 (previously presented) An apparatus for self-initiated instruction issuing comprising:

an instruction queue operable for issuing at least one instruction to an execution unit, said queue including a plurality of entries, each queue entry having a first portion and a second portion, said first portion operable for storing a first link data value and said second portion operable for storing a first data value, said first portion comprising a link mask and said first link data value indicating a target instruction which of the queue's plurality of entries that a dispatching dependent instruction will occupy, wherein said first data value in a first queue entry is set in response to a first link data value in a preselected second queue entry, wherein at least one instruction is selected for issuing in response to a predetermined first data value in a corresponding queue entry;

a rename register device coupled to said queue, said rename register device including a plurality of entries, each entry having a first portion operable for storing a pointer data value and a second portion operable for storing a validity data value, wherein each said pointer data value is associated with a corresponding queue entry, wherein each said first link data value is set in response to said pointer data values and said validity data values, wherein each said rename register device entry includes a third portion operable for receiving a plurality of operand tags, and wherein each said pointer data value is operable for selection in response to a preselected one of said plurality of operand tags, wherein each said queue entry includes a third portion coupled to said rename register device for receiving a first one of said plurality of

operand tags, and a fourth portion coupled to said rename register device for receiving a second one of said plurality of operand tags, wherein said first and second operand tags are associated with a dispatching instruction, and wherein said first operand tag is further associated with said first link data value, wherein said queue is operable for broadcasting a preselected first operand tag; and

a storage device operable for receiving said broadcasting of said first operand tag, wherein each said rename register device entry includes a fourth portion operable for storing a second data value, said second data value being operable for setting in response to an issuing instruction.

Claim 11 (original) The apparatus of claim 10 wherein said first data value is operable for setting in response to said second data value.

Claim 12 (previously presented) The apparatus of claim 10 each said queue entry further comprises a fifth portion operable for storing a second link data value and a sixth portion operable for storing a second data value, and a seventh portion coupled to said rename register device for receiving a third one of said plurality of operand tags, said third operand tag being associated with said dispatching instruction, and wherein said third operand tag is further associated with said second link data value, and wherein said second data value in said first queue entry is set in response to a preselected second link data value in a third queue entry.

Claim 13 (original) The apparatus of claim 12 wherein each said second link data value is set in response to said pointer data values and said validity data values.

Claims 14-52 (cancelled)